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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/533,330

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Stephen Najda

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EXAMINER

FOX, BRANDON C

ART UNIT

PAPER NUMBER

2818

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PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/533,330	<b>Applicant(s)</b> NAJDA, STEPHEN	
	<b>Examiner</b> BRANDON FOX	<b>Art Unit</b> 2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 02 May 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☐ Claim(s) \_\_\_\_\_ is/are rejected.
- 7) ☒ Claim(s) 1-23 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)            | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | Paper No(s)/Mail Date. _____                                      |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>08/09/2005 &amp; 10/17/2007</u> .                             | 6) <input type="checkbox"/> Other: _____                          |

### **DETAILED ACTION**

This is a Non-Final office action based on application 10/533,330 filed May 2, 2005.

Claims 1-23 are currently pending and have been considered below.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 5, 8, 15, 21, 22, & 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Thompson (Pre-Grant Publication 2002/0127752).

**Regarding claims 1-3 & 23**, Thompson disclose a method for modifying the band-gap energy of a semiconductor device comprising:

- Forming a first relatively high quality epitaxial layer (Fig. 1 & 5, 13) on a substrate (11 & 120) wherein the high quality layer including a series of sub-layers of barrier layers (17 & 107) and quantum well layers (16 & 106) (See Paragraph [0020]).
- Forming a second, relatively lower quality, epitaxial defect layer (20 & 112/102) on top of the high quality layer wherein Thompson disclose the defects are provided from a layer or layers such as the two defect layers (112 & 102) shown in Fig. 5 (See Paragraph [0004] & [0030]).

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- Thermally processing using RTA/rapid thermal annealing to effect at least partial diffusion of the defect from the defect layer into the high quality layer in order to achieve quantum well intermixing in the structure (See Paragraphs [0020] & [0030]).

**Regarding claim 5 & 15,** Thompson further discloses:

- Forming a SiO<sub>2</sub> cap layer (not shown) on top of the NT-InP defect layer (102). (See Paragraph [0025]).

**Regarding claim 8,** Thompson further discloses:

- Forming the InP defect layer by means of a reduced temperature MBE/molecular beam epitaxy, such that an abundance of point defect are provided in the InP layer (See Claim 14).

**Regarding claim 21,** Thompson further discloses:

- The annealing is performed at various temperatures in the range of 600-780 degrees C (See Paragraph [0023]).

**Regarding claim 22,** Thompson further discloses:

- The semiconductor device comprises a laser device (See Paragraph [0020]).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Thompson (Pre-Grant Publication 2002/0127752).

**Regarding claim 4**, Thompson discloses a method for modifying the band-gap energy of semiconductor device comprising:

- Forming a quantum well structure and a defect layer on top of the quantum well structure wherein a annealing step is performed to diffuse the defect from the defect layer into the quantum well structure to modify the band-gap energy.

Although Thompson does not disclose a further high quality layer on top of the defect layer prior to the thermal step it would have been obvious to those having ordinary skill in the art to form another high quality layer/quantum well structure on top of the defect layer because laser and LED semiconductor devices commonly comprises of a plurality quantum well regions within a single device to produce different wavelengths of light, therefore by forming another quantum well structure on top of the defect layer when the annealing process is performed

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defects from the defect layer can alter the band-gap energy of more than one quantum well region at the same time during a single annealing step.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Thompson (Pre-Grant Publication 2002/0127752) in view of Yokozeki (US Patent 6,898,224).

**Regarding claim 6**, Thompson discloses all of the limitations of claim 5 (addressed above). Thompson does not disclose the cap layer is adapted to inhibit oxidation. However, Yokozeki discloses a semiconductor laser device comprising:

- Encapsulating the laser device in order to prevent the oxidation of facets (Col. 14, Lines 61-63).

Further since Thompson discloses a cap layer can be formed on the defect layer, it has been held that the recitation that an element is “adapted to” perform a function is not a positive limitation but only requires the ability to so perform. It does not constitute a limitation in any patentable sense. *In re Hutchinson*, 69 USPQ 138.

Claims 7-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thompson (Pre-Grant Publication 2002/012775) in view of Valster (US Patent 5,358,897).

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**Regarding claims 7 & 12**, Thompson discloses all of the limitation of claim 1 (addressed above). Thompson does not disclose varying the source element during growth away from ideal or stoichiometric to result in crystalline defects. However Valster discloses a radiation emitting semiconductor device comprising:

- Forming a plurality Group III-V layer to form the semiconductor device wherein the ratio of III and V during growth is chosen to lie between approximately 100 and 400 which is equivalent to a ratio range of 1:1 to 4:1 or 1:0.25 (See Valster Col. 4, Lines 45-68 & Col. 5, Lines 1-6).

It would have been obvious to those having ordinary skill in the art at the time of invention to incorporate the teachings of Valster with that of Thompson because by varying the ratio of the Group III and V element within that range was favorable for obtaining the greatest possible disorder in the mixed crystals of the semiconductor layer formed (Valster Col.5, Lines 1-6).

**Regarding claims 9-11**, Thompson and Valster discloses all of the limitations of claim 7 (addressed above). Although Thompson does not expressly disclose the defect layer having a defect density in excess of  $1000 \text{ defects/cm}^2$  or  $10^6 \text{ defects/cm}^3$  or the defect layer having a defect density being 10 times or 100 times higher than that of the high quality. However Thompson does disclose a method of for modifying the band-gap of a laser device by having a defect layer formed above a quantum well structure wherein the defect layer has a high

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number of defects in comparison to the quantum well structure which essentially has a no or a low amount of defects present. Therefore it would have been obvious to those having ordinary skill in the art to have the defect layer having a high defect density, such as 1000 defects/cm<sup>2</sup> or 10<sup>6</sup> defects/cm<sup>3</sup>, compared to that of the quantum well structure to thereby allow for the band-gap energy of the quantum well to be more effectively changed.

Claims 13 & 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thompson (Pre-Grant Publication 2002/0127752) in view of Marsh (Pre-Grant Publication 2003/0021313).

**Regarding claims 13 & 14,** Thompson further discloses:

- Subjecting the laser device to a photolithographic patterning/etching step (See Paragraph [0020] & [0030]).

Thompson does not expressly disclose photo-lithographically processing the substrate to spatially define areas of the defect layer over the surface of the substrate or the defect layer is defined over the region of the structure that will form non-absorbing mirrors of a laser device. However Marsh discloses a semiconductor laser device comprising:

- A Silica/SiO<sub>2</sub> layer (Fig. 5, 32) that will serve to form the defects/intermixed region in the waveguide core (16) including quantum



wells (24) wherein the silica layer is spatially patterned over the substrate (12).

- Marsh further discloses a first and second portion are intermixed regions as shown in Figures 4, 5, & 6, wherein both the first and second intermixed portions/regions can serve as NAMs/non-absorbing mirrors (See Marsh Paragraph [0035]).

It would have been obvious to those having ordinary skill in the art at the time of invention to incorporate the teaching of Marsh with that of Thompson because by spatially patterning will serve to control where the intermixed region within the quantum well will be located. Also by forming non-absorbing mirrors the laser device will have high output power at the device facets and the non-absorbing mirror can also serve to prevent a reduction in the band-gap and thereby avoid absorption (See Marsh Paragraph [0061]).

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Thompson (Pre-Grant Publication 2002/0127752) in view Ooi (pre-Grant Publication 2002/0072142).

**Regarding claim 16,** Thompson discloses all of the limitations of claim 1 (addressed above). Thompson does not expressly disclose the defect layer having a different thermal expansion coefficient than the high quality layer/quantum well region to

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create a localized strain. However, Ooi discloses a shifting the band-gap energy of a quantum well layer comprising:

- Forming a stress inducing mask layer on a quantum well structure wherein the stress inducing layer is made from a material having a significant difference in thermal expansion coefficient from the quantum well material (See Ooi Paragraph [0077]).

It would have been obvious to those having ordinary skill in the art at the time of invention to incorporate the teachings of Ooi with that of Thompson because the difference in thermal expansion coefficient will allow significant stress to be created to form a vertical stress field lines that will aid in guiding the migration of point defects to the quantum well structure during the annealing step (See Ooi Paragraph [0078]).

Claims 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thompson (Pre-Grant Publication 20020127752) in view Ooi (Pre-Grant Publication 2002/0072142) as applied to claim 16 above, and further in view of Petroff (US Patent 5,192,709).

**Regarding claims 17-20,** Thompson and Ooi discloses all of the limitations of claims 1 & 16 (addressed above). Thompson discloses forming the quantum well region and the defect layer from Group III and V elements. While Petroff discloses forming a semiconductor device comprising:

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- A GaAs quantum well structure (Fig. 3a, 14) and a AlGaAs donor implantation layer (12b) wherein a strain/de-channeling layer (28) is included in the donor layer (See Petroff Col. 2, Lines 41-66).

It would have been obvious to those having ordinary skill in the art at the time of invention to incorporate the teachings of Petroff with that of Thompson because the strain layer incorporated in the donor implantation serves to help the ions quickly strike and displace lattice atoms within the quantum well structure during the annealing process and will also help to locate the ions with greater precision (Petroff Abstract & Col. 2, Lines 41-66). Further although Thompson, Ooi, and Petroff does not specifically disclose each material as claim in claims 17-19, they do disclose the layer of the semiconductor device is made from Group III and V elements therefore it would have obvious to those having ordinary skill in the art at the time of invention to use these material to form the defect and high quality layers since laser and LED structures are commonly formed from Group III-V ternary and quaternary alloy layers.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BRANDON FOX whose telephone number is (571)270-5016. The examiner can normally be reached on Mon - Fri 6:30 - 5:00 EST.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached on 571-272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

BCF  
3/27/2009

/DAVID VU/  
Primary Examiner, Art Unit 2818

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